26nm 32Gb based e-NAND product Family

Document Title
e-NAND

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft.	Feb. 16. 2011	
0.2	Added the side ball pitch (7. PKG Mechanical Drawing)	Mar. 22. 2011	
0.3	Updated the 8GB eMMC Register data	Mar. 25. 2011	
0.4	Updated the Device Register data	Mar. 29. 2011	
1.0	Released 1.0 ver.	Mar. 31.2011	
1.1	- Updated the 3.1.1 Pin Assignments - Corrected the Creg from 1.1uF ->0.1uF (Table 5.) - Added the typical active current	Apr. 13. 2011	

Features

■ Packaged NAND flash memory with MultiMediaCard interface

■ High capacity memory access

■ eMMC/MultiMediaCard system specification, compliant with V4.41

■ Full backward compatibility with previous MultiMediaCard system specification

■ Bus mode
- High-speed MultiMediaCard protocol.
- Three different data bus widths: 1 bit, 4 bits,8 bits.
- Data transfer rate: up to 104Mbyte/s
- DDR mode supported

■ Operating voltage range:
- V_{CCQ} = 3.3V/1.8V
- V_{CC} = 3.3 V

■ Error free memory access
- Internal error correction code
- Internal enhanced data management algorithm (wear levelling, bad block management, garbage collection)
- Possibility for the host to make sudden power failure safe-update operations for data content

■ Security
- Password protection of data
- Security Erase
- Security Trim
- Secure bad block management
- Built-in write protection

■ Boot
- Simple boot sequence method

■ Power saving
- Enhanced power saving method by introducing sleep functionality

■ Partition management with enhanced storage.

■ Hardware reset supported

Device summary

Capacities	Root part number	Package	PKG Size
4GB	H26M31001FPR	FBGA153	11.5 X 13 X 0.8 mm
8GB	H26M42001FMR	FBGA153	11.5 X 13 X 1.0 mm
16GB	H26M54001DQR	FBGA169	12.0 X 16 X 1.0 mm
32GB	H26M68001CFR	FBGA169	12.0 X 16 x 1.2 mm

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1. Description

The Hynix e-NAND is an embedded flash memory storage solution with MultiMediaCard™ interface (eMMC™). The eMMC™ was developed for universal low cost data storage and communication media. The Hynix e-NAND is fully compatible with MMC bus and hosts.

The Hynix e-NAND communications are made through an advanced 11-pin bus.
The bus can be either 1-bit, 4-bit, or 8-bit in width. The device operates in high-speed mode at clock frequencies equal to or higher than 20MHz, which is the MMC standard. The communication protocol is defined as a part of this MMC standard and referred to as MultiMediaCard mode.

The device is designed to cover a wide area of applications such as smart phones, cameras, organizers, PDA, digital recorders, MP3 players, pagers, electronic toys, etc. They feature high performance, low power consumption, low cost and high density.

To meet the requirements of embedded high density storage media and mobile applications, the Hynix e-NAND supports both 3.3V supply voltage (V_{CC}), and 3.3V/1.8V input/output voltage (V_{CCQ}).

The address argument for the Hynix e-NAND is the sector address (512-byte sectors) instead of the byte address. This means that Hynix e-NAND is not backward compatible with devices of density lower than 2 Gbytes. If there is no indication by the host to the memory that the host is capable of handling sector type of addressing, the Hynix e-NAND will change its state to inactive.

The device has a built-in intelligent controller which manages interface protocols, data storage and retrieval, wear leveling, bad block management, garbage collection, and
internal ECC.

The Hynix e-NAND makes available to the host sudden power failure safe-update operations for the data content, by supporting reliable write features.

The device supports boot operation with enhance area and sleep/awake commands.
In particular, during the sleep state the host power regulator for VCC can be switched off, thus minimizing the power consumption of the Hynix e-NAND.

1.1 e-NAND Standard Specification

The Hynix e-NAND device is fully compatible with the JEDEC Standard Specification No. JESD84-A441.
This datasheet describes the key and specific features of the Hynix e-NAND device. Any additional information required to interface the device to a host system and all the practical methods for card detection and access can be found in the proper sections of the JEDEC Standard Specification.

2. System features

The following list identifies the main features of the MultiMediaCard System, which:

- Is targeted for portable and stationary applications
- Has these System Voltage (VDD) Ranges:

	Voltage
Communication	1.7 - 1.95 or 2.7 - 3.6
Memory Access	2.7 - 3.6

- Is designed for read-only, read/write and I/O cards
- Supports card clock frequencies of 0-20MHz, 0-26MHz or 0-52MHz
- Has a maximum data rate up to 832Mbits/sec.
- Has a defined minimum performance
- Maintains card support for three different data bus width modes: 1-bit (default), 4-bit, and 8-bit
- Includes definition for higher than 2GB of density of memories
- Includes password protection of data
- Supports basic file formats for high data interchangeability
- Includes application specific commands
- Enables correction of memory field errors
- Has built-in write protection features for the boot and user areas, which may be permanent,power-on, or temporary
- Includes a simple erase mechanism
- Maintains full backward compatibility with previous MultiMediaCard systems
- Provides a possibility for the host to make sudden power failure safe-update operations for the data content.
- Enhanced power saving method by introducing a sleep functionality.
- Introduces Boot Operation Mode to provide a simple boot sequence method.
- Provides a new CID Register setting to recognize *e-NAND*.
- Obsoletes the SPI Mode.
- Defines I/O voltage (VCCQ) and core voltage (VCC) separately for *e-NAND*.
- Defines Erase-unit size and Erase timeout for high-capacity memory.
- Provides access size register indicating one (or multiple) programmable boundary unit(s) of device.
- Obsoletes the Absolute Minimum Performance.
- Introduces *e-NAND* OCR setting and response.
- Defines WP group size for high-capacity devices.
- Introduces Alternate Boot Operation Mode.
- Introduces Secure Erase & Trim to enhance data security.
- Supports Multiple User Data Partition with Enhanced User Data Area options
- Signed access to a Replay Protected Memory Block.
- Introduces dual data rate transfer.
- Introduces high speed boot.
- Enhanced Write Protection with Permanent and Partial protection options.
- Introduces hardware reset signa.

2.1 Operating Conditions

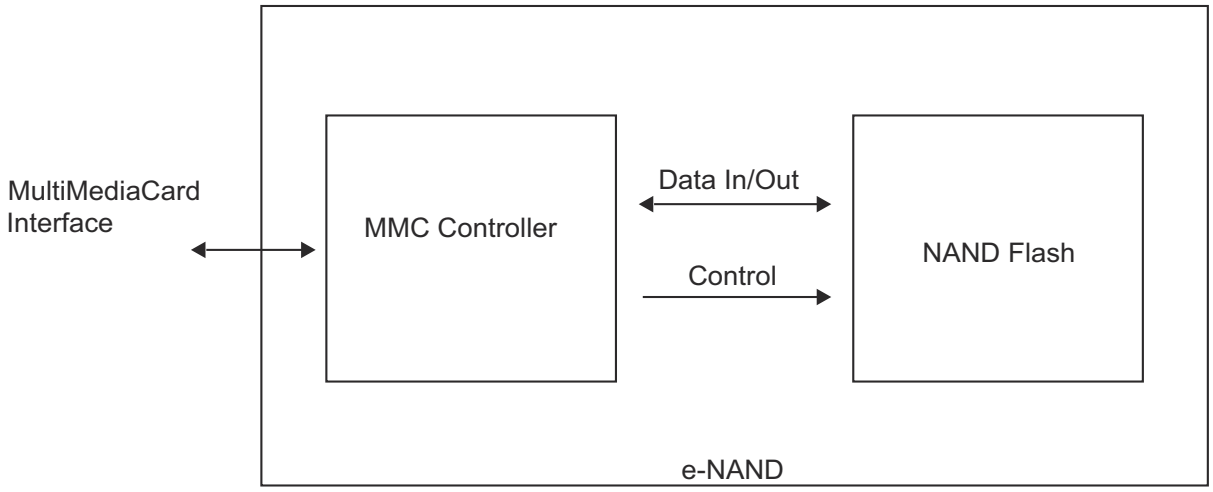
Temperature	Operating	-25℃~85℃
	Non-Operating	-40℃~85℃

3. Device physical description

The Hynix e-NAND contains a single chip controller and flash memory module, see the below *Figure 1 Device block diagram.* The microcontroller interfaces with a host system allowing data to be written to and read from the flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

Figure2 shows the package connections. See *Table1: Signal names* for the description of the signals corresponding to the balls.

Figure 1: Device block diagram



3.1 Package connections

3.1.1 Pin Assignments

1.The ball corresponding to V_{DDI} must be decoupled with an external capacitance.

Figure 2-1: FBGA153 package connections (top view through package)

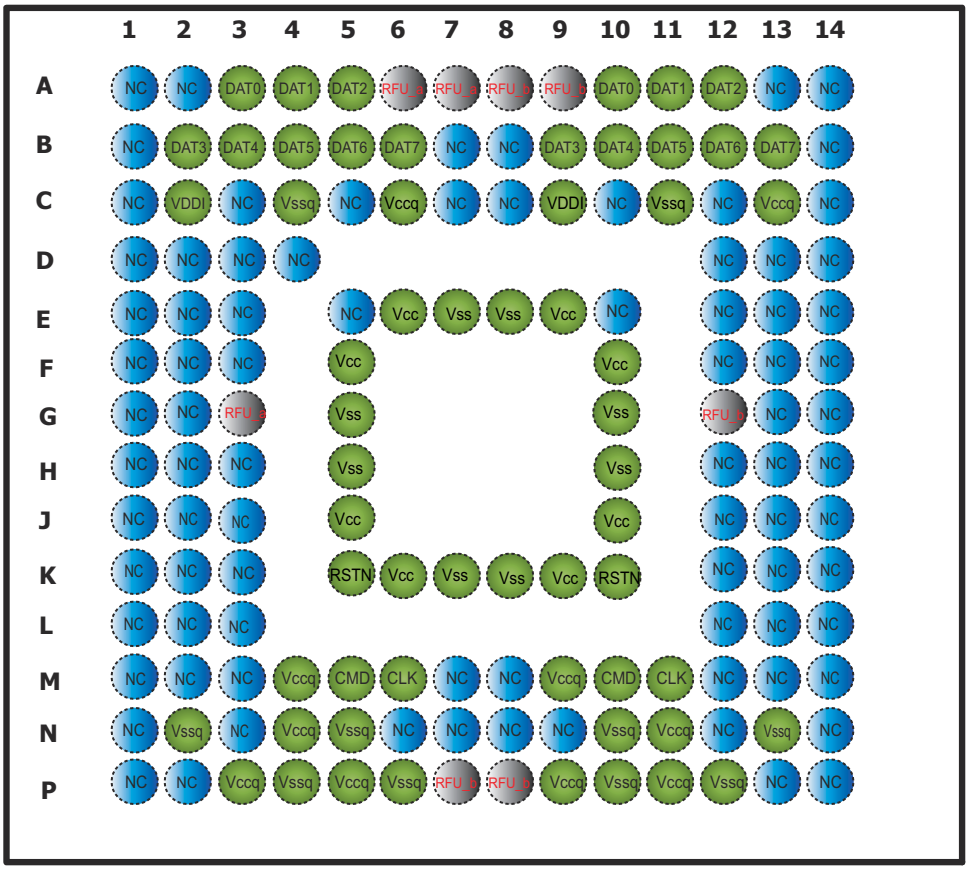
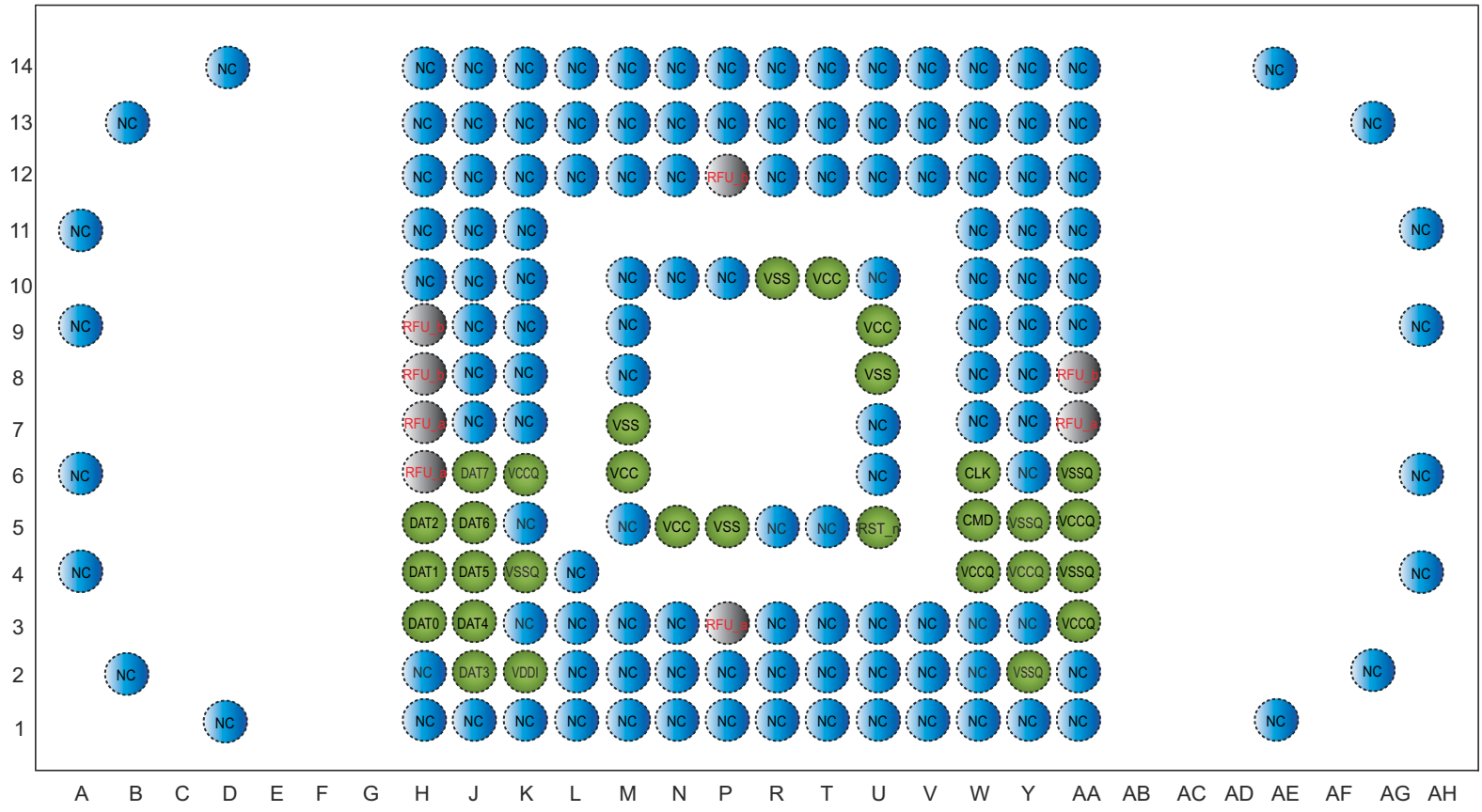


Figure 2-2: FBGA169 package connections (top view through package)



3.2 Form factor

The ball diameter, d, and the ball pitch, p, for the FBGA153/169 package are

- **d = 0.30mm (solder ball diameter)**
- **p = 0.5mm (ball pitch)**

Figure 3:

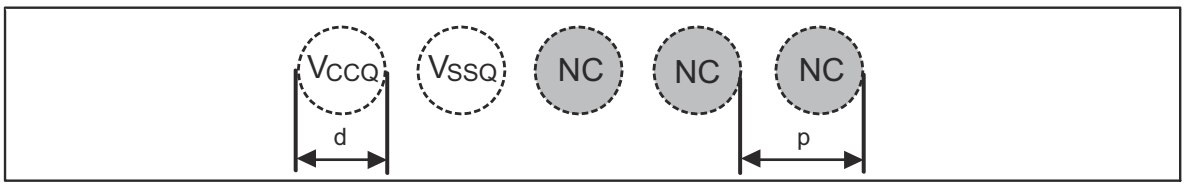


Table 1-1 : FBGA153 Pin Description

Pins	e-NAND Interface		
	Name	IO Type(1)	Description
M5	CMD	I/O/PP/OD	Command / Response
M6	CLK	I	Clock
G5, E7, K8, H10	Vss	S	Flash Memory Supply Voltage Ground
C4, N2, N5, P4, P6	Vssq	S	Core Supply Voltage Ground
C6, M4, N4, P3, P5	Vccq	S	Core Supply Voltage
E6, F5, K9, J10	Vcc	S	Flash Memory Supply Voltage
A3	DATA0	I/O/PP	Data
A4	DAT1	I/O/PP	Data
A5	DAT2	I/O/PP	Data
B2	DAT3	I/O/PP	Data
B3	DAT4	I/O/PP	Data
B4	DAT5	I/O/PP	Data
B5	DAT6	I/O/PP	Data
B6	DAT7	I/O/PP	Data
C2	V_{DDI}	-	The capacitor (1μF) must be connected for internal power stability.
K5	RST_n	I	Reset signal pin
RFU	Reserved for Future Use		
NC	Not Connected		
DNU	Do Not Use		

Note:
1. S: Power Supply; I: input; O: output; PP: push-pull; OD: open-drain;
2. The DAT0-DAT7 pins for read-only cards are output only

Table 1-2 : FBGA169 Pin Description

Pins	e-NAND Interface		
	Name	IO Type(1)	Description
W5	CMD	I/O/PP/OD	Command / Response
W6	CLK	I	Clock
M7, P5, R10, U8	Vss	S	Flash Memory Supply Voltage Ground
K4, Y2, Y5, AA4, AA6	Vssq	S	Core Supply Voltage Ground
K6, W4, Y4, AA3, AA5	Vccq	S	Core Supply Voltage
M6, N5, T10, U9	Vcc	S	Flash Memory Supply Voltage
H3	DATA0	I/O/PP	Data
H4	DAT1	I/O/PP	Data
H5	DAT2	I/O/PP	Data
J2	DAT3	I/O/PP	Data
J3	DAT4	I/O/PP	Data
J4	DAT5	I/O/PP	Data
J5	DAT6	I/O/PP	Data
J6	DAT7	I/O/PP	Data
K2	V_{DDI}	-	The capacitor (1㎌) must be connected for internal power stability.
U5	RST_n	I	Reset signal pin
RFU	Reserved for Future Use		
NC	Not Connected		
DNU	Do Not Use		

Note:
1. S: Power Supply; I: input; O: output; PP: push-pull; OD: open-drain;
2. The DAT0-DAT7 pins for read-only cards are output only

4. MultiMediaCard interface

The signal/pin assignments are listed in *Table1.* Refer to this table in conjunction with *Figure2* and *Figure3: Form factor.*

4.1 Signals description

4.1.1 Clock (CLK)

The Clock input, CLK, is used to synchronize the memory to the host during command and data transfers. Each clock cycle gates one bit on the command and on all the data lines. The Clock frequency, fPP, may vary between zero and the maximum clock frequency.

4.1.2 Command (CMD)

The CMD signal is a bidirectional command channel used for device initialization and command transfer. The CMD signal has two operating modes: open-drain and push-pull.
The open-drain mode is used for initialization, while the push-pull mode is used for fast command transfer. Commands are sent by the MultiMediaCard bus master (or host) to the device who responds by sending back responses.

4.1.3 Input/outputs (DAT0-DAT7)

DAT0 to DAT7 are bidirectional data channels. The signals operate in push-pull mode. The Hynix e-NAND includes internal pull ups for all data lines. These signals cannot be driven simultaneously by the host and the Hynix e-NAND device. Right after entering the 4-bit mode, the card disconnects the internal pull ups of lines DAT1 and DAT2. Correspondingly right after entering the 8-bit mode, the card disconnects the internal pull ups of lines DAT1, DAT2 and DAT4-DAT7.By default, after power-up or hardware reset, only DAT0 is used for data transfers. The host can configure the device to use a wider data bus, DAT0, DAT0-DAT3 or DAT0-DAT7, for data transfer.

4.1.4 VCC core supply voltage

VCC provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase). The core voltage (VCC) can be within 2.7V and 3.6V.

4.1.5 VSS ground

Ground, VSS, is the reference for the power supply. It must be connected to the system ground.

4.1.6 VCCQ input/ output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}. The input/output voltage (V_{CCQ}) can be either within 1.65/1.7V and 1.95V (low voltage range) or 2.7V and 3.6V (high voltage range).

4.1.7 VSSQ supply voltage

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}.

4.1.8 Reset

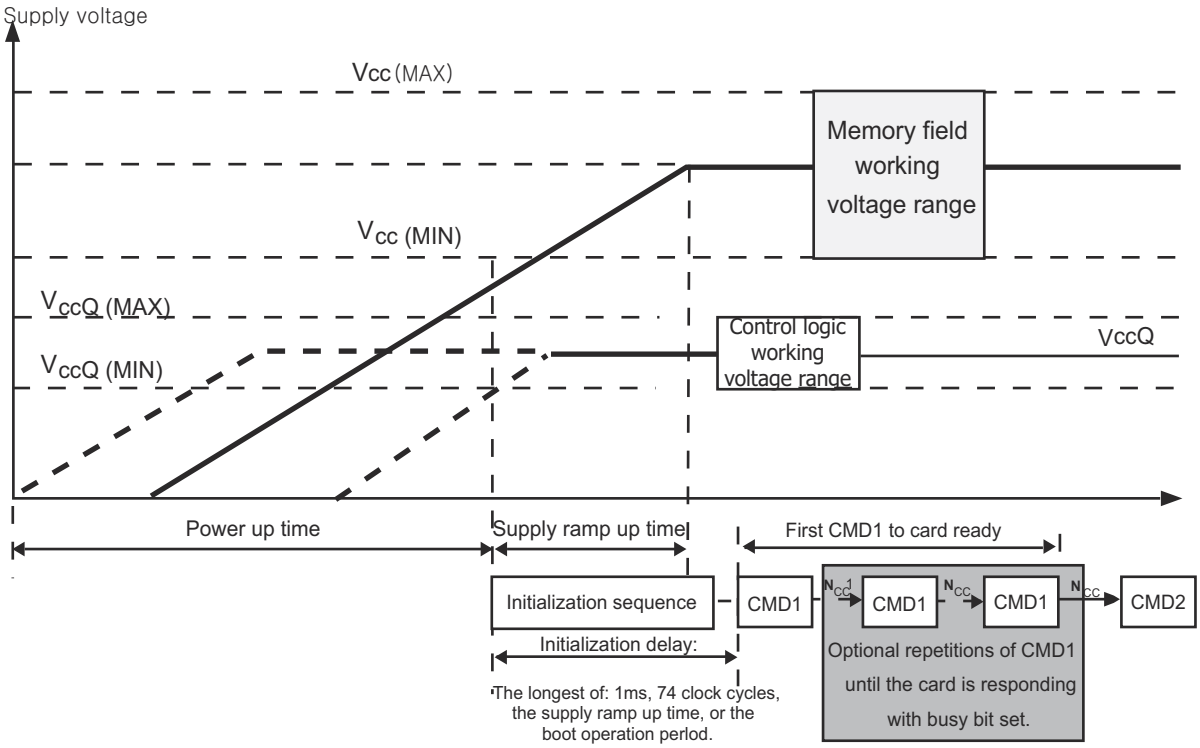
Reset signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. Host need to set bit[0:1] in the extended CSD register [162] to 0x1 to enable this functionality before the host uses.

4.2 Bus Topology

The Hynix e-NAND device supports the MMC protocol. For more details, refer to section 6.4 of the JEDEC Standard Specification No. JESD84-A441. The section 12 of the JEDEC Standard Specification contains a bus circuitry diagram for reference.

4.3 Power up

Figure 3: e-NAND power-up diagram



An *e-NAND* power-up must adhere to the following guidelines:

• When power-up is initiated, either VCC or VCCQ can be ramped up first, or both can be ramped up simultaneously.

• After power up, the *e-NAND* enters the *pre-idle* state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.

• If the *e-NAND* does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, the *e-NAND* moves immediately to the *idle* state. While in the *idle* state, the *e-NAND* ignores all bus transactions until CMD1 is received. If the *e-NAND* supports only specification v4.2 or earlier versions, the device enters the *idle* state immediately following power-up.

• If the BOOT_PARTITION_ENABLE bit is set, the *e-NAND* moves to the *pre-boot* state, and the *e-NAND* waits for the boot-initiation sequence. Following the boot operation period, the *e-NAND* enters the *idle* state. During the *pre-boot* state, if the *e-NAND* receives any CMD-line transaction other than the boot initiation sequence (keeping CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA) and CMD1, the *e-NAND* moves to the *Idle* state. If *e-NAND* receives theboot initiation sequence (keeping the CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA), the *e-NAND* begins boot operation. If boot acknowledge is enabled, the *e-NAND* shall send acknowledge pattern "010" to the host within the specified time. After boot operation is terminated, the *e-NAND* enters the *idle* state and shall be ready for CMD1 operation. If the *e-NAND* receives CMD1 in the *pre-boot* state, it begins responding to the command and moves to the card identification mode.

• While in the *idle* state, the *e-NAND* ignores all bus transactions until CMD1 is received.

• CMD1 is a special synchronization command used to negotiate the operation voltage range and to poll the device until it is out of its power-up sequence. In addition to the operation voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 1 second of the first CMD1 issued with a valid OCR range.

• If the *e-NAND* device was successfully partitioned during the previous power up session (bit 0 of EXT_CSD byte [155] PARTITION_SETTING_COMPLETE successfully set) then the initialization delay is (instead of 1s) calculated from INI_TIMEOUT_PA (EXT_CSD byte [241]). This timeout applies only for the very first initializastion after successful partitioning. For all the consequtive initialization 1sec timeout will apply.

• The bus master moves the device out of the *idle* state. Because the power-up time and the supply ramp up time depend on application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

• After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.

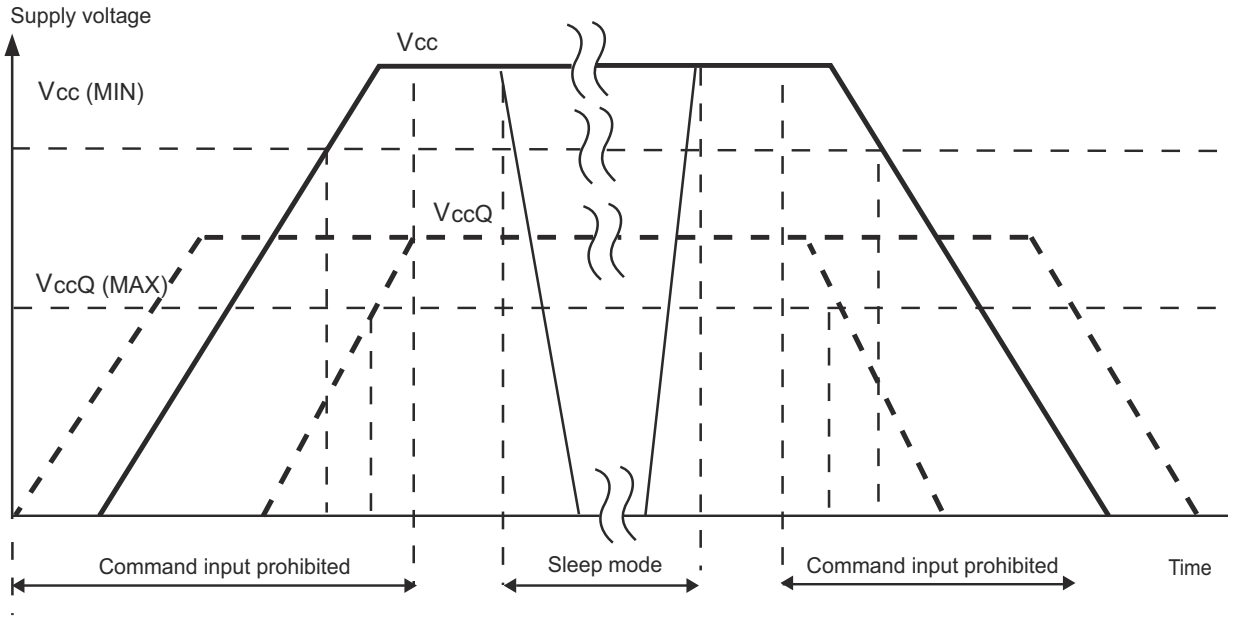
• Every bus master must implement CMD1.

4.4 e-NAND power cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit.

If VCC or VCCQ are below 0.5 V for longer than 1 ms, the slave shall always return to the *pre-idle* state,and perform the appropriate boot behavior, as appropriate. The slave will behaves as in a standard powerupcondition once the voltages have returned to their functional ranges.

Figure 4: e-NAND power cycle



4.5 Bus operating conditions

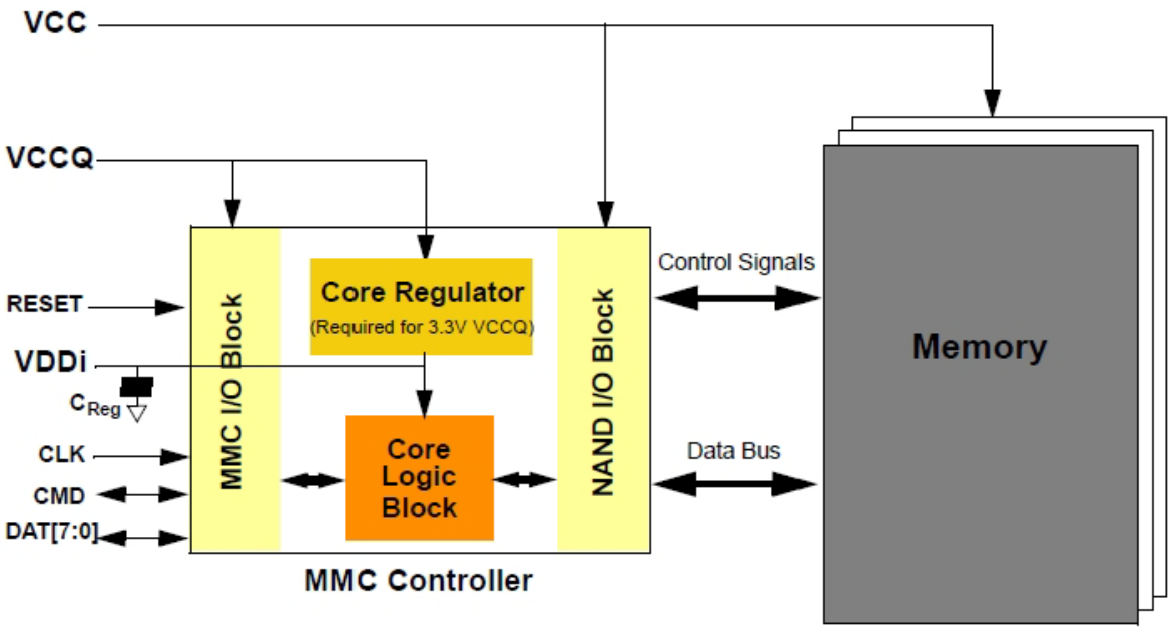
Table 2 : General operation conditions

Parameter		Symbol	Min	Max.	Unit	Remark
Peak voltage on lines	fBGA		-0.5	VccQ+0.5	V	
All Inputs						
Input Leakage Current (before initialization sequenceand/or the internal-pull up resistors connected)			-100	100	μA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)			-2	2	μA	
All Inputs						
Output Leakage CurrentCurrent (before initialization sequence)			-100	100	μA	
Output Leakage Current (after initialization sequence)			-2	2	μA	

4.5.1 Power supply

In the *e-NAND*, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage shown in Figure 62. The core regulator is optional and only required when VCCQ is in the 3V range. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

Figure 5: e-NAND internal power diagram



The *e-NAND* supports one or more combinations of VCC and VCCQ as shown in Table. The VCCQ must be defined at equal to or less than VCC.

Table 3 : e-NAND power supply voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply voltage (NAND)	Vcc	2.7	3.6	V	
Supply voltage (I/O)	Vccq	2.7	3.6	V	
		1.65	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V	tPRUL		25	ms	

The *e-NAND* must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations

Table 4 : e-NAND voltage combinations

		VCCQ	
		1.65V~1.95V	2.7V~3.6V
VCC	2.7V~3.6V	Valid	Valid

4.5.2 Bus signal line load

The total capacitance C_L of each line of the e-NAND bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{BGA} of the card connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{BGA}$$

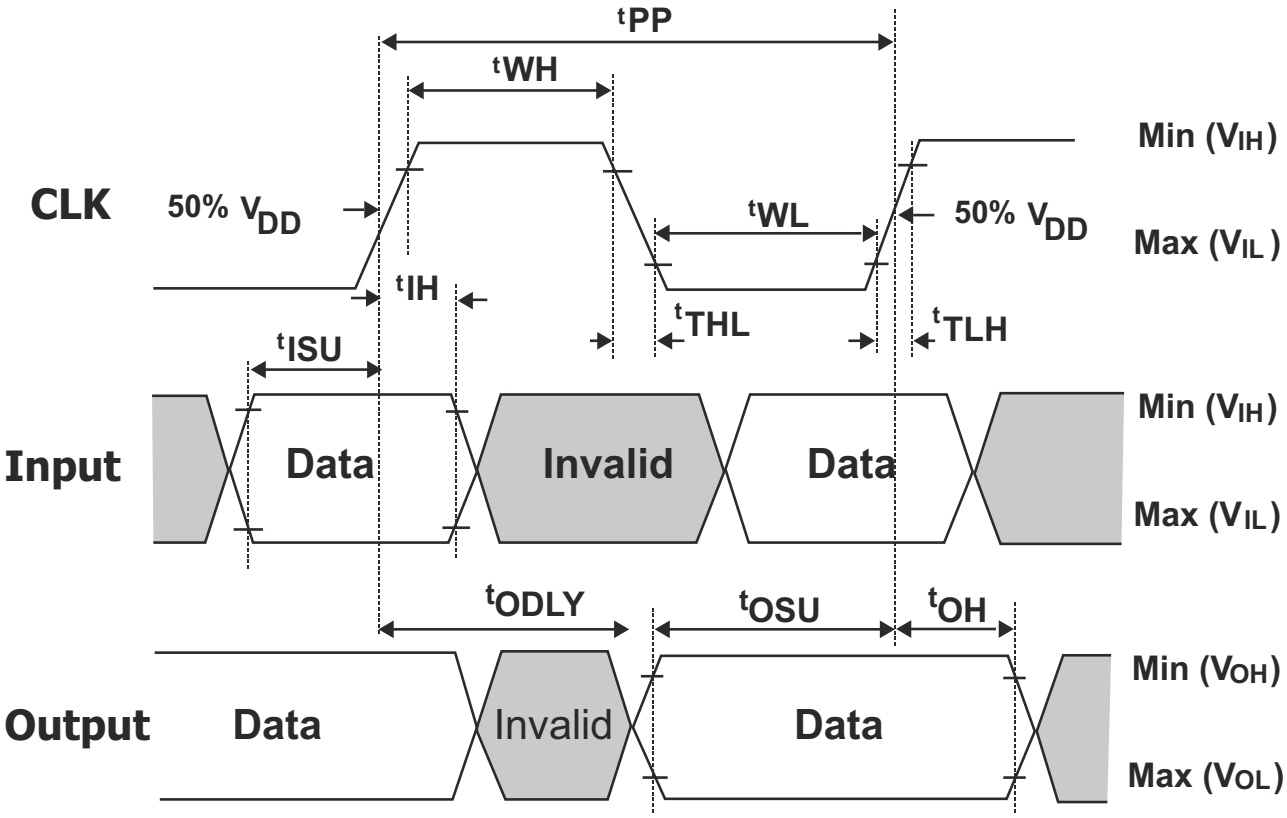
and requiring the sum of the host and bus capacitances not to exceed 20 pF:

Table 5 : e-NAND Capacitance

Parameter	Symbol	Min	Max.	Recommand	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	kohm	to prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10	50	50	kohm	to prevent bus floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	50	kohm	It is not necessary to put pull-up resistance on RST_n(H/W reset) line if host does not use H/W reset.
Impedence on CLK/CMD/ DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_CLK	0	47	22	ohm	
Serial's resistance on CMD/ DAT0~7 Line	SR_CMD SR_DAT 0~7	0	47	0	ohm	
VDDQ Capacitor value	C1 & C2	2.2 + 0.1	4.7 + 0.22	2.2 +0.1	uF	Coupling capacitor should be connected with VDDQ and VSSQ as closely as possible
VDD Capacitor value($\leq$ 8GB)	C3 & C4	2.2 + 0.1	4.7 + 0.22	2.2 +0.1	uF	Coupling capacitor should be connected with VDD and VSS as closely as possible
VDD Capacitor value($\geq$ 8GB)	C3 & C4	2.2 + 0.1	4.7 + 0.22	4.7+0.22	uF	
VDDi capacitor value	C_{reg}	1	4.7 + 0.1	0.1	uF	Coupling capacitor should be connected with VDDi and VSSi as closely as possible

4.6 Bus timing

Figure 6: Timing diagram: data input/output



Data must always be sampled on the rising edge of the clock.

4.6.1 Card interface timings

Table 6 : High-speed card interface timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	C_L <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock rise time[4]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	C_L <= 30 pF
Output hold time	t_{OH}	2.5		ns	C_L <= 30 pF
Signal rise time[5]	t_{rise}		3	ns	C_L <= 30 pF
Signal fall time	t_{fall}		3	ns	C_L <= 30 pF

NOTE 1. CLK timing is measured at 50% of VDD.
NOTE 2. A MultiMediaCard shall support the full frequency range from 0-26Mhz, or 0-52MHz
NOTE 3. Card can operate as high-speed card interface timing at 26 MHz clock frequency.
NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).
NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 7 : Backward-compatible card interface timing

Parameter	Symbol	Min	Max.	Unit	Remark(1)
Clock CLK(2)					
Clock frequency Data Transfer Mode (PP)(3)	f_{PP}	0	26	MHz	CL <= 30 pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock low time	t_{WL}	10		ns	CL <= 30 pF
Clock rise time(4)	t_{TLH}		10	ns	CL <= 30 pF
Clock fall time	t_{THL}		10	ns	CL <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	CL <= 30 pF
Input hold time	t_{IH}	3		ns	CL <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time(5)	t_{OSU}	11.7		ns	CL <= 30 pF
Output hold time(5)	t_{OH}	8.3		ns	CL <= 30 pF

NOTE 1. The card must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

NOTE 2. CLK timing is measured at 50% of VDD.

NOTE 3. For compatibility with cards that support the v4.2 standard or earlier, host should not use > 20 MHz before switching to high-speed interface timing.

NOTE 4. CLK rise and fall times are measured by min (VIH) and max (VIL).

NOTE 5. tOSU and tOH are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.

Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the systemor to use slow clock frequency, so that host could have data set up margin for those devices.
In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its' application notes.

4.7 Bus timing for DAT signals during 2X data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. the CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 12.7, therefore there is no timing change for the CMD signal.

Figure 7: Timing diagram: data input/output in dual data rate mode

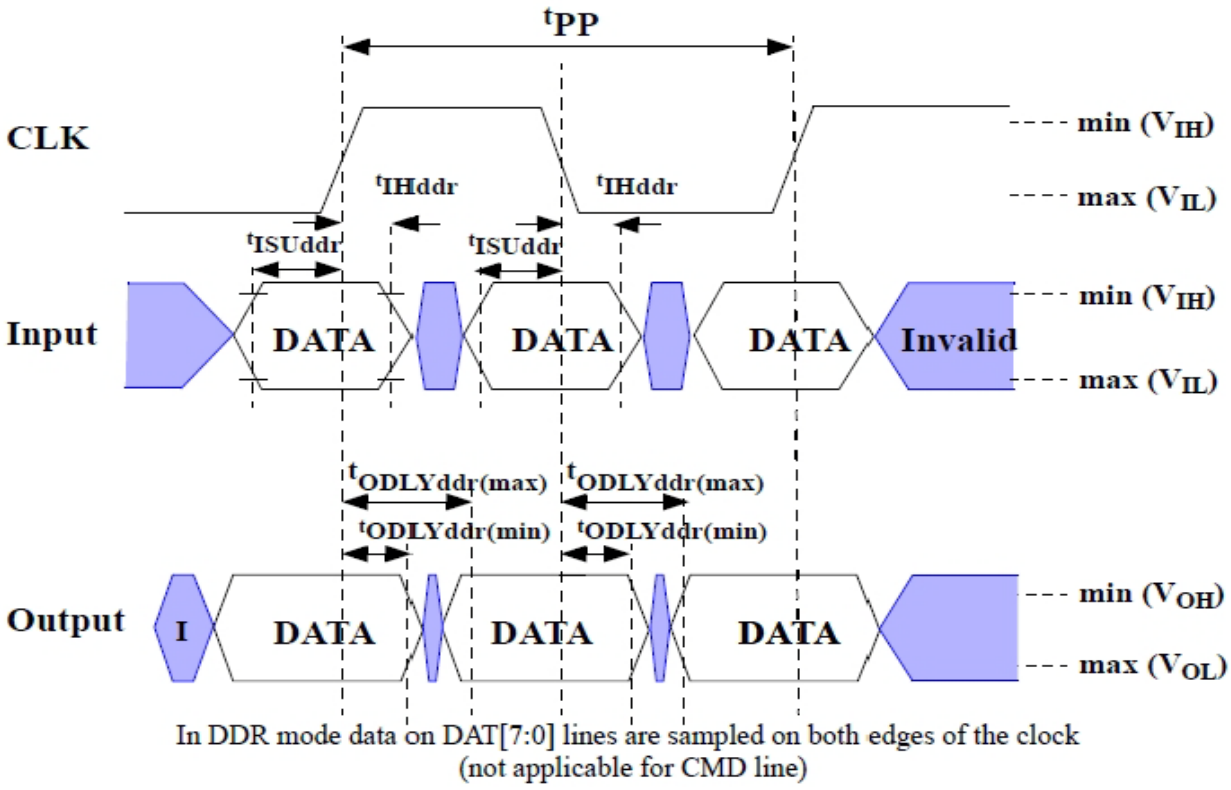


Table 8 : Dual data rate interface timings

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK(1)					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Inputs CMD, DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUDDR}	2.5		ns	C_L <= 20 pF
Input hold time	t_{IHDDR}	2.5		ns	C_L <= 20 pF
Outputs CMD, DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYDDR}$	1.5	7	ns	C_L <= 20 pF
Signal rise time(all signal)2	t_{RISE}		2	ns	C_L <= 20 pF
Signal fall time (all signal)	t_{FALL}		2	ns	C_L <= 20 pF

NOTE 1. CLK timing is measured at 50% of VDD.

NOTE 2. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL)

5. MultimediaCard functional description

All communication between the host and the device is controlled by the host (master). The following section provides an overview of the identification and data transfer modes, commands, dependencies, various operation modes and restrictions for controlling the clock signal. For detailed information, refer to section 7 of the JEDEC Standard Specification No. JESD84-A441.

5.1 General

All communication between host and card is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

• Broadcast commands

Broadcast commands are intended for all cards in a MultiMediaCard system2. Some of these commands require a response.

• Addressed (point-to-point) commands

The addressed commands are sent to the addressed card and cause a response from this card.

• Boot mode

The card will be in boot mode after power cycle, reception of CMD0 with arguement of 0xF0F0F0F0 or (*e*-NAND only) assertion of hardware reset signal.

• Card identification mode

The card will will be in card identification mode after boot operation mode is finished or if host and /or card does not support boot operation mode. The card will be in this mode, until the SET_RCA command (CMD3) is received.

• Interrupt mode

Host and card enter and exit interrupt mode simultaneously. In interrupt mode there is no data transfer.
The only message allowed is an interrupt service request from the card or the host.

• Data transfer mode

The card will enter data transfer mode once an RCA is assigned to it. The host will enter data transfer mode after identifying the card on the bus.

• Inactive mode

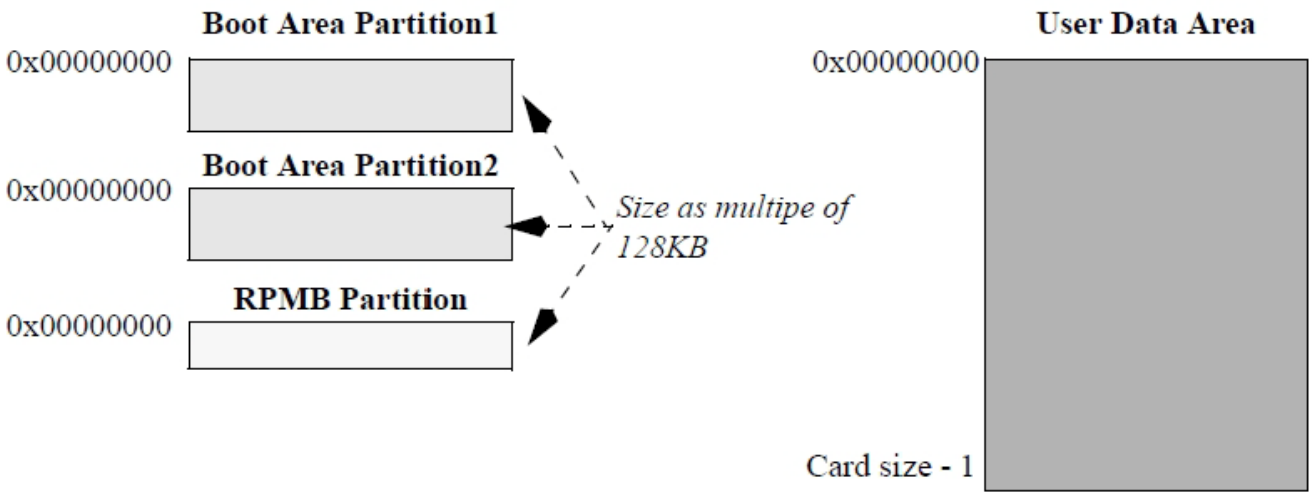
The card will enter inactive mode mode either card operating voltage range or access mode is not valid. The card can also enter inactive mode with Go_INACTIVE_STATE command (CMD15). The card will reset to *Pre-idle* state with power cycle.

5.2 Partition Management

The default area of the memory device consists of a User Data Area to store data, two possible boot area partitions for booting and the Replay Protected Memory Block Area Partition to manage data in an authenticated and replay protected manner. For detailed information regarding Command restrictions, configure partitions and Access partitions , refer to section 7.2 of the JEDEC Standard Specification No. JESD84-A441 .

The memory configuration initially consists (before any partitioning operation) of the User Data Area and RPMB Area Partitionsm and Boot Area Partitions (whose dimensions and technology features are defined by Hynix).

Figure 8: e-NAND memory organization at time zero



The embedded device offers also the possibility of configuring by the host additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block Area scan be classified as follows:

- Two Boot Area Partitions, whose size is multiple of 128 KB and from which booting from *e-NAND* can be performed.
- One RPMB Partition accessed through a trusted mechanism, whose size is defined as multiple of 128 KB.
- Four General Purpose Area Partitions to store sensitive data or for other host usage models and whose size is multiple of a Write Protect Group.

Each of the General Purpose Area Partitions can be implemented with enhanced technological features (such as better reliability*) that distinguish them from the default storage media. If the enhanced storage media feature is supported by the device, boot and RPMB Area Partitions shall be implemented as enhanced storage media by default.

Boot and RPMB Area Partitions' sizes and attributes are defined by the memory manufacturer (read-only), while General Purpose Area Partitions' sizes and attributes can be programmed by the host only once in the device life-cycle (one-time programmable).

5.3 Boot operation mode

In boot operation mode, the master (MultiMediaCard host) can read boot data from the slave (e-NAND device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For detailed information regarding card reset to Pre-idle state, boot partition, boot operation, alternative boot operation, access boot partition, boot bus width and data access configuration and boot partition write protection refer to section 7.3 of the JEDEC Standard Specification No. JESD84-A441 .

5.4 Card identification mode

While in card identification mode the host resets the card, validates operation voltage range and access mode, identifies the card and assigns a Relative Card Address (RCA) to the card on the bus. All data communication in the Card Identification Mode uses the command line (CMD) only. For detailed information regarding card reset, operating voltage range validation, access mode validation, From busy to ready and Card identification process, refer to section 7.4 of the JEDEC Standard Specification No. JESD84-A441.

5.5 Interrupt mode

The interrupt mode on the MultiMediaCard system enables the master (MultiMediaCard host) to grant the transmission allowance to the slaves (card) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a card request for service. Supporting MultiMediaCard interrupt mode is an option, both for the host and the card. For detailed information, refer to section 7.5 of the JEDEC Standard Specification No. JESD84-A441.

5.6 Data transfer mode

When the card is in *Stand-by* State, communication over the CMD and DAT lines will be performed in push-pull mode. Until the contents of the CSD register is known by the host, the fPP clock rate must remain at fOD. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g., block length, card storage capacity, maximum clock rate, etc. For detailed information regarding command sets and extended settings, High-speed mode selection, power class selection,bus testing procedure, bus width selection, data read, data write, erase, secure erase, secure trim, TRIM, write protect management, Card lock/unlock operation, application-specific commands, Sleep(CMD5), Replay Protected Memory Block, Dual data rate mode selection and Dual data rate mode operation, refer to section 7.6 of the JEDEC Standard Specification No. JESD84-A441.

5.7 Clock control

The MultiMediaCard bus clock signal can be used by the host to put the card into energy saving mode, or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down. For detailed information refer to section 7.7 of the JEDEC Standard Specification No. JESD84-A441.

5.8 Error conditions

For detailed information refer to section 7.8 of the JEDEC Standard Specification No. JESD84-A441.

5.9 Minimum performance

For detailed information refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A441.

5.10 Commands

For detailed information refer to section 7.10 of the JEDEC Standard Specification No. JESD84-A441.

5.11 State transition

For detailed information refer to section 7.11 and 7.13 of the JEDEC Standard Specification No. JESD84-A441.

5.12 Response

For detailed information refer to section 7.12 of the JEDEC Standard Specification No. JESD84-A441.

5.13 Memory array partitioning

The basic unit of data transfer to/from the e-NAND is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.
For block oriented commands, the following definition is used:

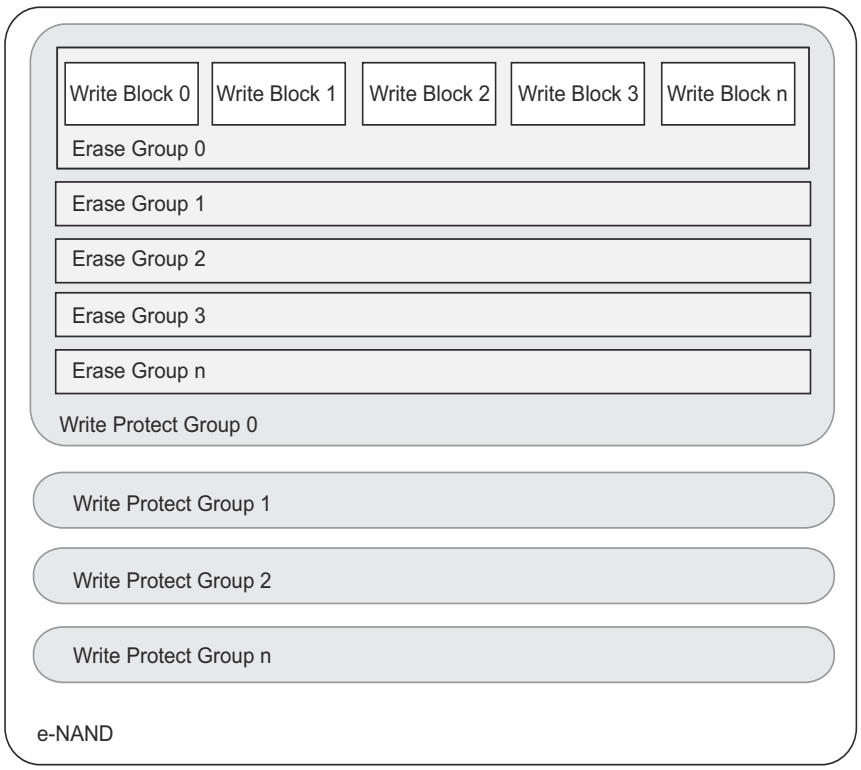
• **Block**: is the unit which is related to the block oriented read and write commands. Its size is the number of bytes which will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.

For R/W cards, special erase and write protect commands are defined:

• The granularity of the erasable units is the **Erase Group:** The smallest number of consecutive write blocks which can be addressed for erase. The size of the Erase Group is card specific and stored in the CSD when ERASE_GROUP_DEF is disabled, and in the EXT_CSD when ERASE_GROUP_DEF is enabled.

• The granularity of the Write Protected units is the **WP-Group:** The minimal unit which may be individually write protected. Its size is defined in units of erase groups. The size of a WP-group is card specific and stored in the CSD when ERASE_GROUP_DEF is disabled, and in the EXT_CSD when ERASE_GROUP_DEF is enabled.

Figure 9: Memory array partitioning



5.14 Timings

For detailed information refer to section 7.15 of the JEDEC Standard Specification No. JESD84-A441.

6. Device registers

There are five different registers within the device interface:

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (driver stage register)
- Extended card specific data register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands (refer to section 8 of the JEDEC Standard Specification No. JESD84-A441. The device does not implement the DSR register.

The MultiMediaCard has a status register to provide information about the device current state and completion codes for the last host command.

6.1 Operation conditions register (OCR)

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the card and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by all cards. For detailed information, refer to section 8.1 of the JEDEC Standard Specification No. JESD84-A441.

If the host tries to change the OCR values during an initialization procedure the changes in the OCR content will be ignored.

The level coding of the OCR register is as follows:

- Restricted voltage windows = Low
- Device busy = Low

Table 9 : OCR register definition

OCR bit	Description	MultiMediaCard
6 to 0	Reserved	000 0000b
7	V_{CCQ}	1b
14 to 8	2.0 - 2.6	000 0000b
23 to 15	2.7 - 3.6 (High VCCQ range)	1 1111 1111b
28 to 24	Reserved	000 0000b
30 to 29	Access mode	10b (sector mode)
31	Power-up status bit (busy)(1)	

1. This bit is set to Low if the device has not finished the power-up routine.

6.2 Card identification (CID) register

The CID register is 16-byte long and contains a unique card identification number used during the card identification procedure. It is a 128-bit wide register with the content as defined in *Table11*. It is programmed during device manufacturing and can not be changed by MultiMediaCard hosts. For details, refer to section 8.2 of the JEDEC Standard Specification No. JESD84-A441.

Table 10 : Card identification (CID) register

Name	Field	Width	CID - slice	CID - value				Note
				4GB	8GB	16B	32GB	
Manufacturer ID	MID	8	[127:120]	90h				
Reserved		6	[119:114]	00_0000b				
Card/BGA	CBX	2	[113:112]	01b				BGA
OEM/application ID	OID	8	[111:104]	4ah				
Product name	PNM	48	[103:56]	4e495820h				HYNIX
Product revision	PRV	8	[55:48]	5dh				
Product serial number	PSN	32	[47:16]	00002 ab1h	00002 cedh	00002 d30h	TBD	Not Fixed
Manufacturing date	MDT	8	[15:8]					Not Fixed
CRC7 checksum	CRC	7	[7:1]	61h	2eh	1fh	TBD	Not Fixed
Not used, always '1'	Reserved	1	[0:0]	TBD				

6.3 Card specific data register(CSD)

All the configuration information required to access the device data is stored in the CSD register. The MSB bytes of the register contain the manufacturer data and the two least significant bytes contains the host controlled data (the device copy, write protection and the user ECC register).

The host can read the CSD register and alter the host controlled data bytes using the SEND_CSD and PROGRAM_CSD commands.

In *Table12,* the cell type column defines the CSD field as read only (R), one time programmable (R/W) or erasable (R/W/E). The programmable part of the register (entries marked by W or E) can be changed by command CMD27.

The copy bit in the CSD can be used to mark the device as an original or a copy. Once set it cannot be cleared. The device can be purchased with the copy bit set (copy) or cleared, indicating the device is a master.

The one time programmable (OTP) characteristic of the copy bit is implemented in the MultiMediaCard controller firmware and not with a physical OTP cell.

For details, refer to section 8.3 of the JEDEC Standard Specification No. JESD84-A441.

Table 11 : Card specific data register

Name	Field	Width	Cell Type	CID - slice	CID - value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
MultiMediaCard protocol version	SPEC_VERS	4	R	[125:122]	4h
Reserved		2	R	[121:120]	0
Data read access-time-1	TAAC	8	R	[119:112]	4fh
Data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. data transfer rate	TRAN_SPEED	8	R	[103:96]	32h
Command classes	CCC	12	R	[95:84]	f5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved		2	R	[75:74]	0
Device size	C_SIZE	12	R	[73:62]	fffh
Max. read current at VCC(min)	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current at VCC(max)	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current at VCC(min)	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current at VCC(max)	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	7h/fh/1fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved				[20:20]	0
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GROUP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h

Table 12 : Card specific data register (continued)

Name	Field	Width [bits]	Cell Type	CID - slice	CID - value
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code 2 R/W/E none 0	ECC	2	R/W/E	[9:8]	0h
CRC	CRC	7	R/W/E	[7:1]	28h/30h/00h
Not used, always '1'		1	-	[0:0]	1h

6.4 Extended CSD register

The extended CSD register defines the device properties and selected modes. It is 512-byte long. The 320 most significant bytes are the properties segment that defines the device capabilities and cannot be modified by the host. The 192 lower bytes are the modes segment that defines the configuration the device is working in. For details, refer to section 8.4 of the JEDEC Standard Specification No. JESD84-A441.These modes can be changed by the host by means of the Switch command.

Table 13. Extended CSD(1)

Name	Field	Size (bytes)	Cell Type	CID - slice	CID - slice value			
					4GB	8GB	16GB	32GB
Properties segment								
Reserved[1]		7	TBD	[511:505]				
Supported command sets	S_CMD_SET	1	R	[504]	01h			
HPI features	HPI_FEATURES	1	R	[503]	03h			
Background operations support	BKOPS_SUPPORT	1	R	[502]	01h			
Reserved[1]		255	TBD	[501:247]				
Background operations status	BKOPS_STATUS	1	R	[246]	00h			
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	00000000h			
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	6eh	6eh	dah	TBD
Reserved[1]		1	TBD	[240]				
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	00h			
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	00h			
Reserved[1]		2	TBD	[237:236]				
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	00h			

Table 13. Extended CSD(1)(continued)

Name	Field	Size (bytes)	Cell Type	CID slice	CID - slice value			
					4GB	8GB	16GB	32GB
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	00h			
Reserved[1]		1	TBD	[233]				
TRIM Multiplier	TRIM_MULT	1	R	[232]	0fh			
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	15h			
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	06h			
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	09h			
Boot information	BOOT_INFO	1	R	[228]	07h			
Reserved[1]		1	TBD	[227]				
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	10h	10h	20h	TBD
Access size	ACC_SIZE	1	R	[225]	06h	07h	07h	TBD
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	8h	10h	10h	TBD
High_capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	01h			
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	08h			
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	01h	01h	02h	TBD
Sleep current(VCC)	S_C_VCC	1	R	[220]	08h			
Sleep current(VCCQ)	S_C_VCCQ	1	R	[219]	08h			
Reserved[1]		1	TBD	[218]				
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	10h			
Reserved[1]		1	TBD	[216]				
Sector Count	SEC_COUNT	4	R	[215:212]	7380 00h	e740 00h	01d74 000h	TBD
Reserved[1]		1	TBD	[211]				
Minimum Write Performance for 8bit at52MHz	MIN_PERF_W_8_52	1	R	[210]	08h			
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	08h			
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	08h			
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	08h			
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	08h			
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	08h			
Reserved[1]		1	TBD	[204]				
Power class for 26MHz at 3.6V	PWR_CL_26_360	1	R	[203]	00h			
Power class for 52MHz at 3.6V	PWR_CL_52_360	1	R	[202]	00h			

Table 13. Extended CSD(1)(continued)

Name	Field	Size (bytes)	Cell Type	CID slice	CID - slice value			
					4GB	8GB	16GB	32GB
Power class for 26MHz at 1.95V	PWR_CL_26_195	1	R	[201]	00h			
Power class for 52MHz at 1.95V	PWR_CL_52_195	1	R	[200]	00h			
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	01h			
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	02h			
Reserved[1]		1	TBD	[197]				
Card type	CARD_TYPE	1	R	[196]	0Fh			
Reserved[1]		1	TBD	[195]				
CSD structure version	CSD_STRUCTURE	1	R	[194]	02h			
Reserved[1]		1	TBD	[193]				
Extended CSD revision	EXT_CSD_REV	1	R	[192]	05h			
Modes Segment								
Command set	CMD_SET	1	R/W/E_P	[191]	00h			
Reserved[1]		1	TBD	[190]				
Command set revision	CMD_SET_REV	1	R	[189]	00h			
Reserved[1]		1	TBD	[188]				
Power class	POWER_CLASS	1	R/W/E_P	[187]	00h			
Reserved[1]		1	TBD	[186]				
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	00h			
Reserved[1]		1	TBD	[184]				
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	00h			
Reserved[1]		1	TBD	[182]				
Erased memory content	ERASED_MEM_CONT	1	R	[181]	00h			
Reserved[1]		1	TBD	[180]				
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/WE_P	[179]	00h			
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	00h			
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	00h			
Reserved[1]		1	TBD	[176]				
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	00h			

Table 13. Extended CSD(1)(continued)

Name	Field	Size (bytes)	Cell Type	CID slice	CID - slice value			
					4GB	8GB	16GB	32GB
Reserved[1]		1	TBD	[174]				
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	00h			
Reserved[1]		1	TBD	[172]				
User area write protection register	USER_WP	1	R/W,R/W/C_P & R/W/E_P	[171]	00h			
Reserved[1]		1	TBD	[170]				
FW configuration	FW_CONFIG	1	R/W	[169]	00h			
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	10h	10h	20h	TBD
Write reliability setting register	WR_REL_SET	1	R/W	[167]	00h			
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	00h			
Reserved[1]		1	TBD	[165]				
Manually start background operations	BKOPS_START	1	W/E_P	[164]	00h			
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	00h			
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	00h			
HPI management	HPI_MGMT	1	R/W/E_P	[161]	00h			
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	03h			
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	00019Ah	00019Ah	00019Ah	TBD
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	00h			
Paritioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	00h			
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	00h			
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	00h			
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	00h			
Reserved[1]		1	TBD	[135]				
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	00h			
Reserved[1]		1	TBD	[133:0]				

NOTE 1. Reserved bits should read as "0."

6.5 RCA (relative card address)

registerThe writable 16-bit relative card address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-card communication after the device identification procedure. The default value of the RCA register is '0x0001'. The value '0x0000' is reserved to set all cards into the standby statewith CMD7. For details refer to section 8.5 of the JEDEC Standard Specification No. JESD84-A441.

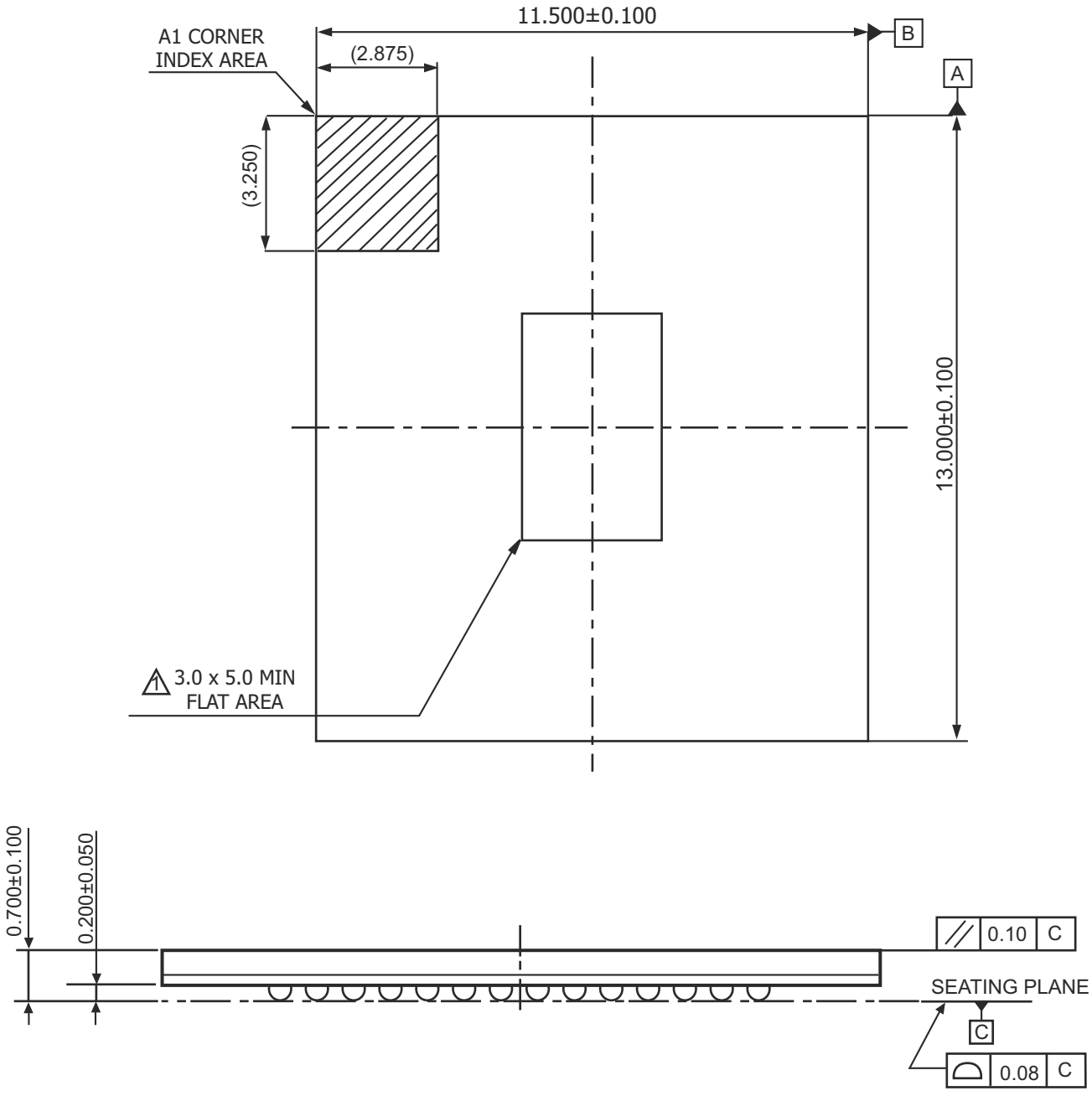
6.6 DSR (driver stage register) register

The 16-bit driver stage register (DSR) can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of devices on the bus). The CSD register contains the information concerning the DSR register usage.

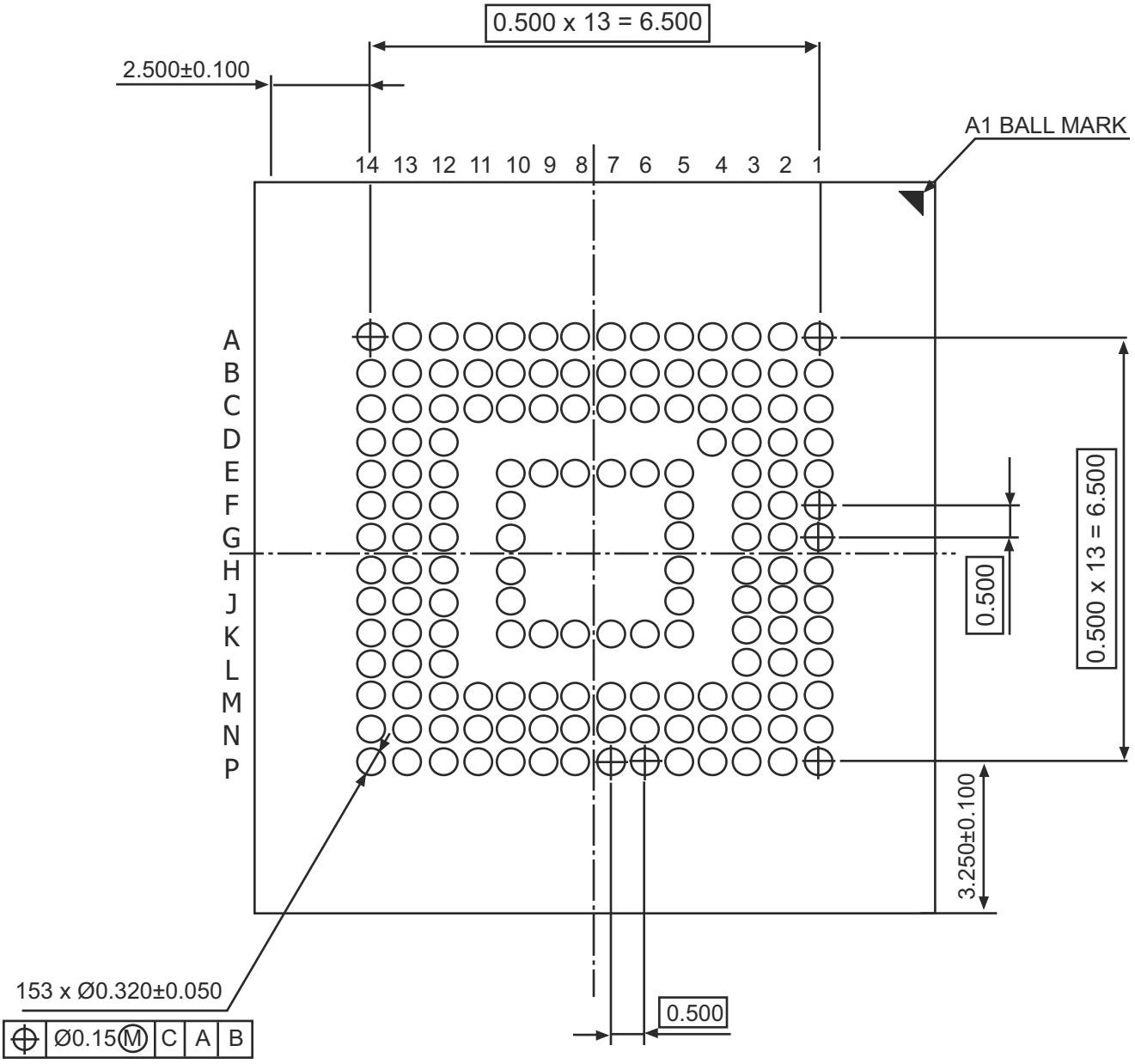
The default value of the DSR register is '0x404'. For details refer to section 8.6 of the JEDEC Standard Specification No. JESD84-A441.

7. PKG Mechanical Drawing

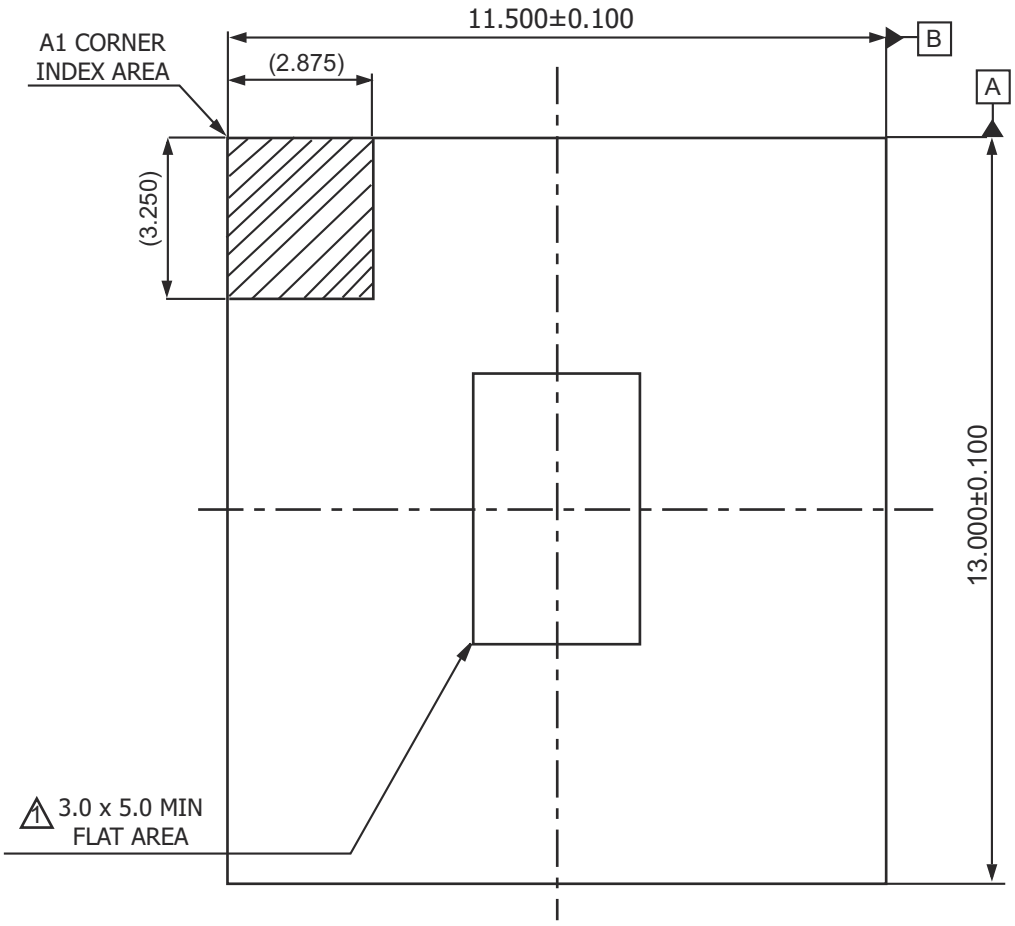
7-1) 11.5X13X0.8 (Top side)

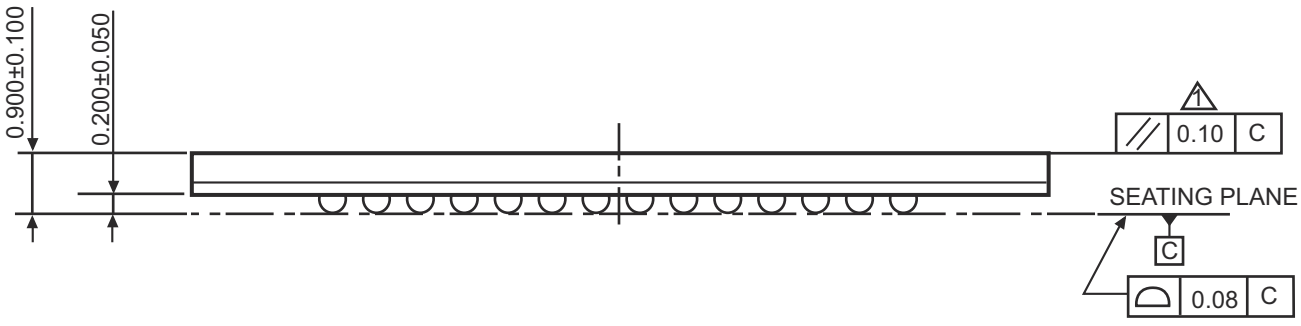


7-1) 11.5X13X0.8 (Bottom side)

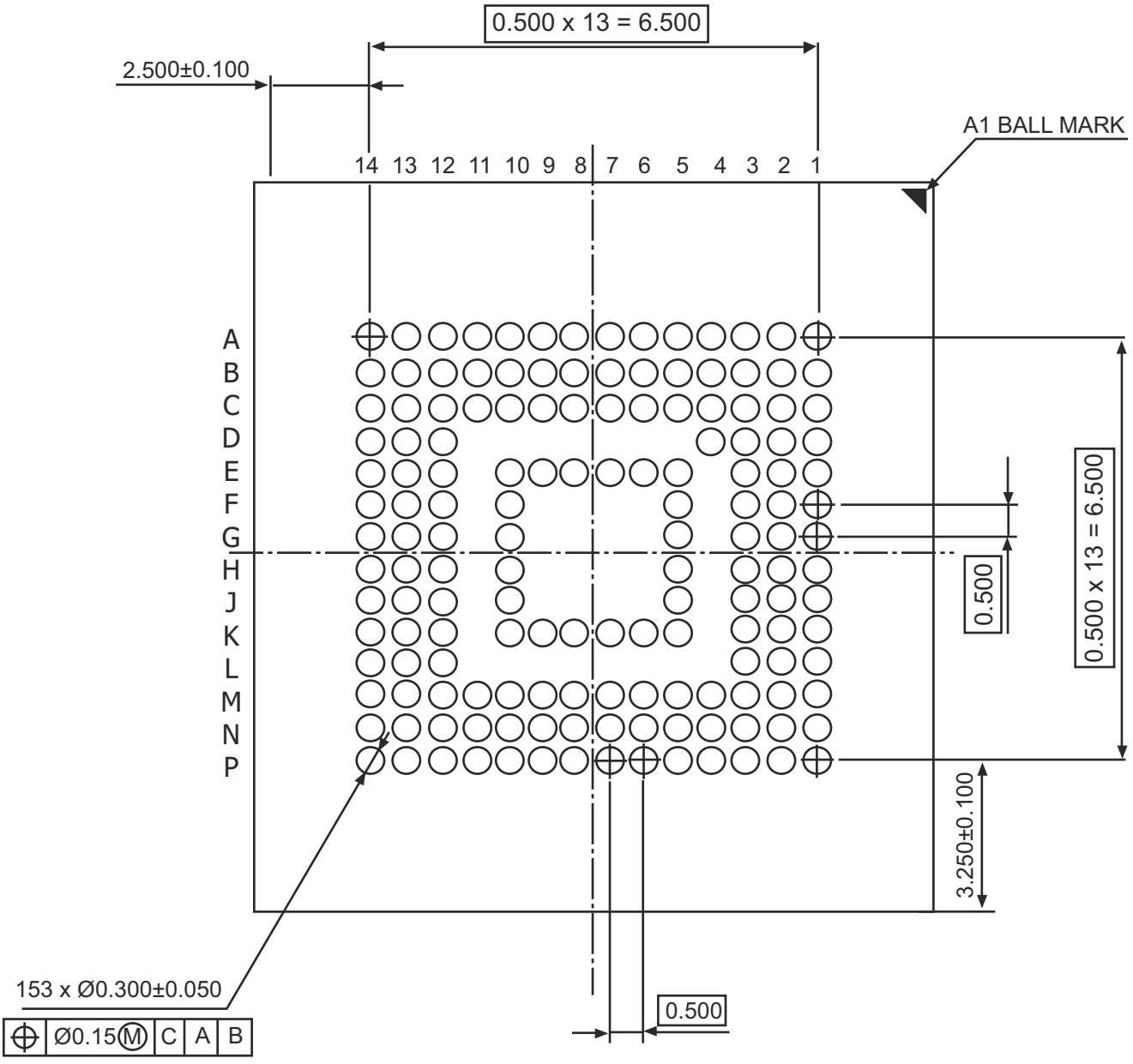


7-2) 11.5X13X1.0 (Top side)

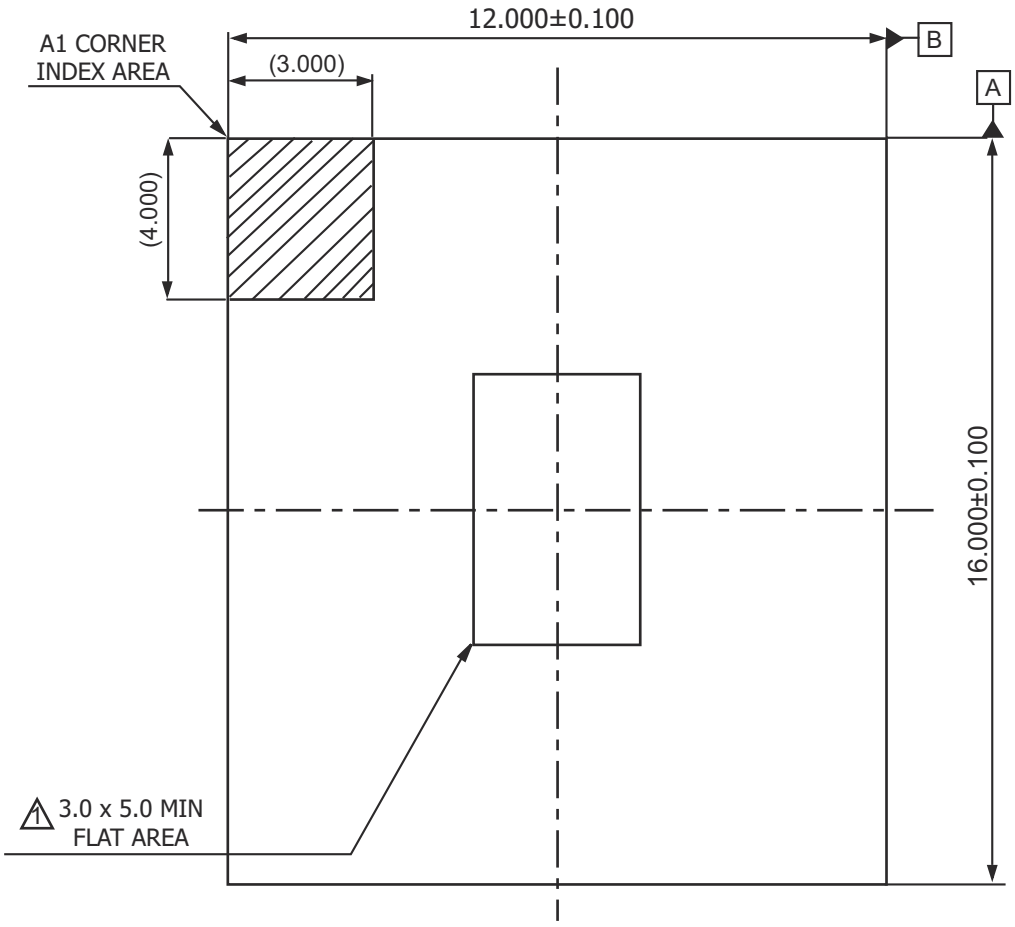


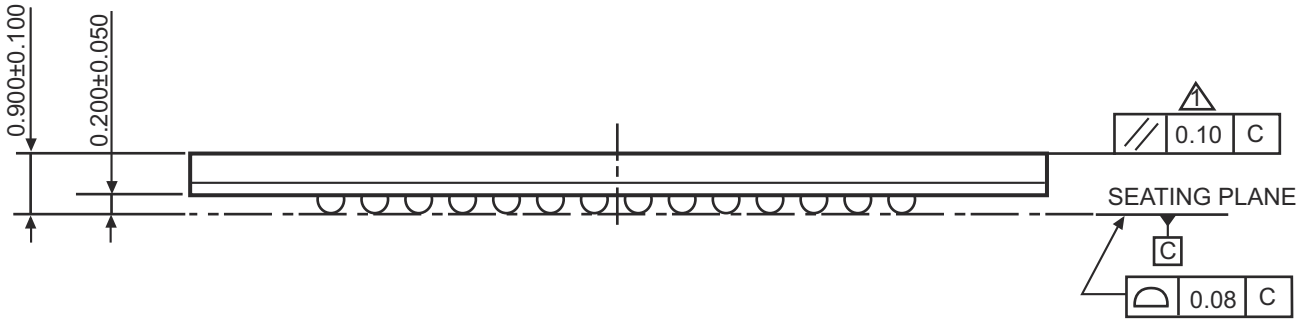


7-2) 11.5X13X1.0 (Bottom side)

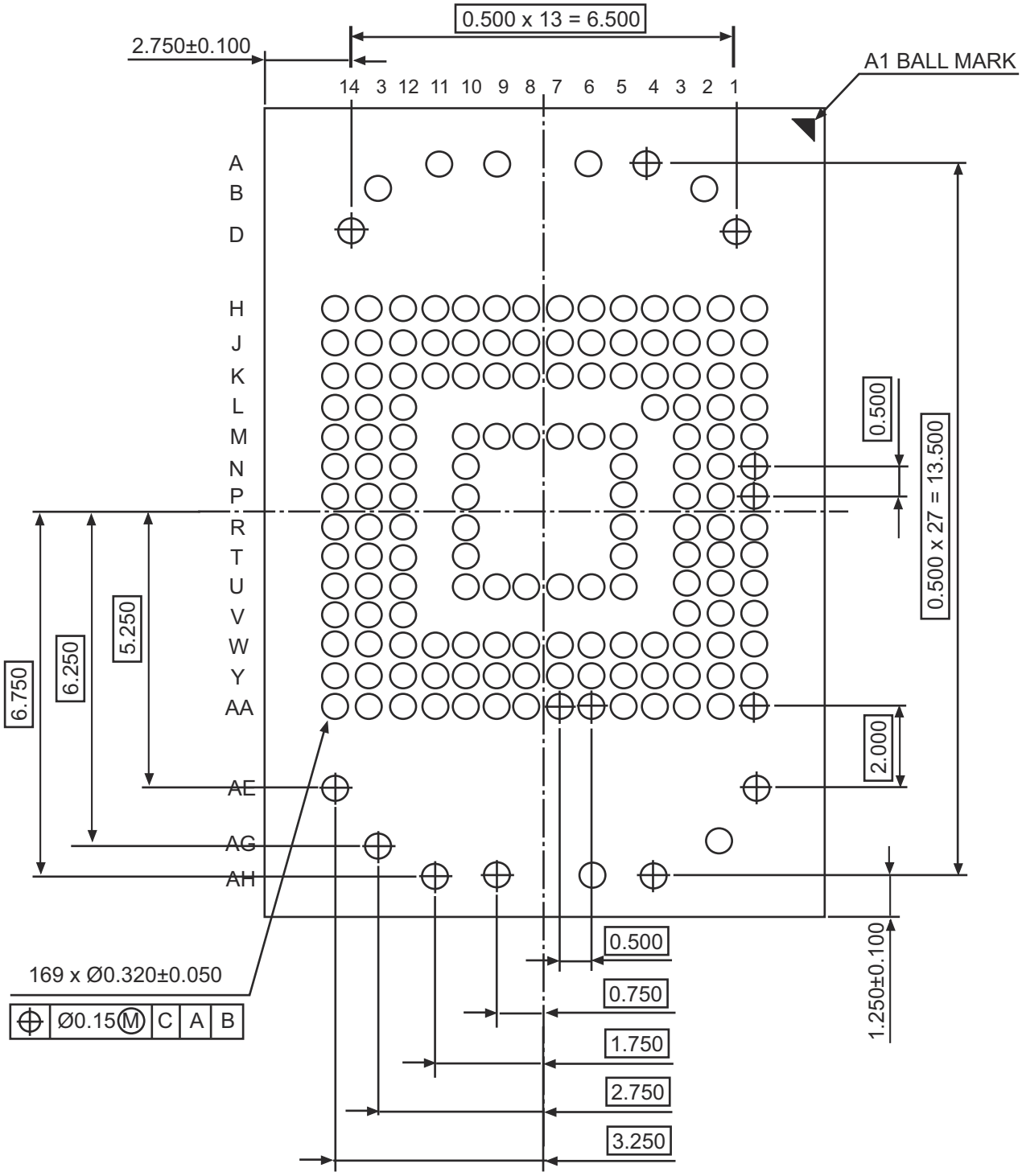


7-3) 12X16X1.0 (Top side)

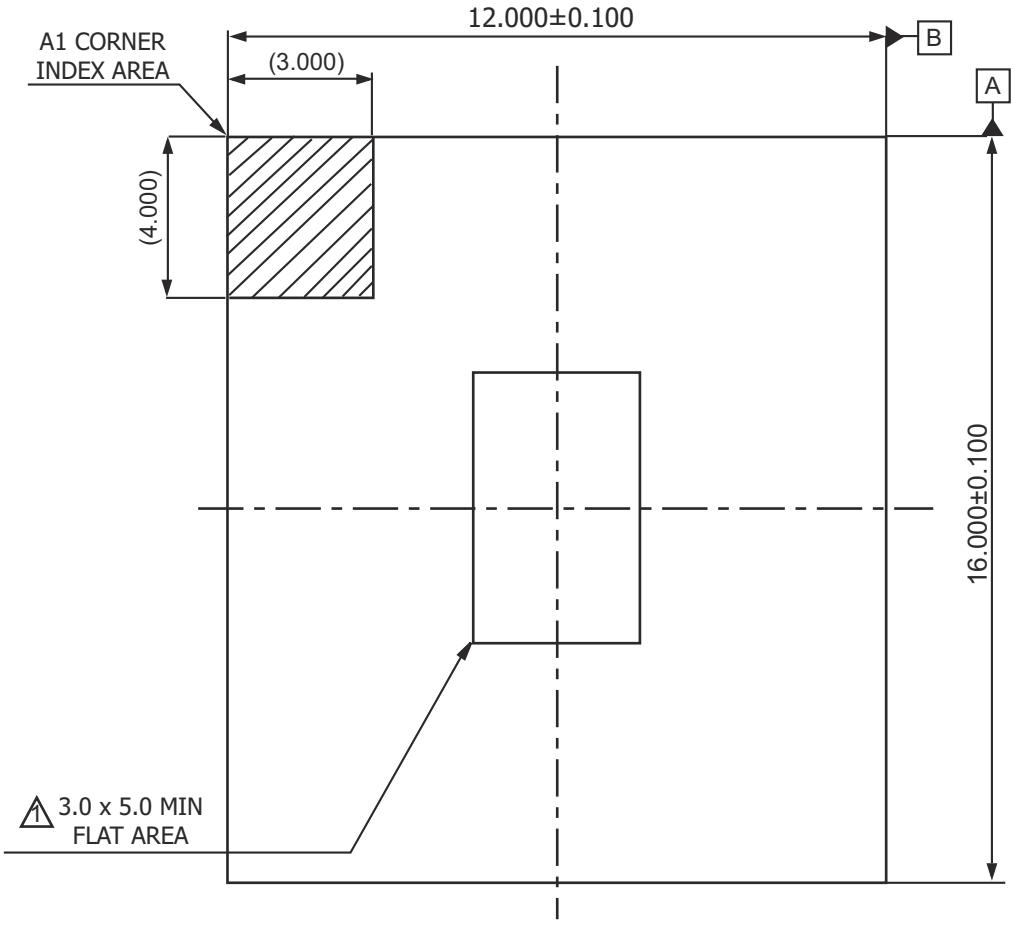


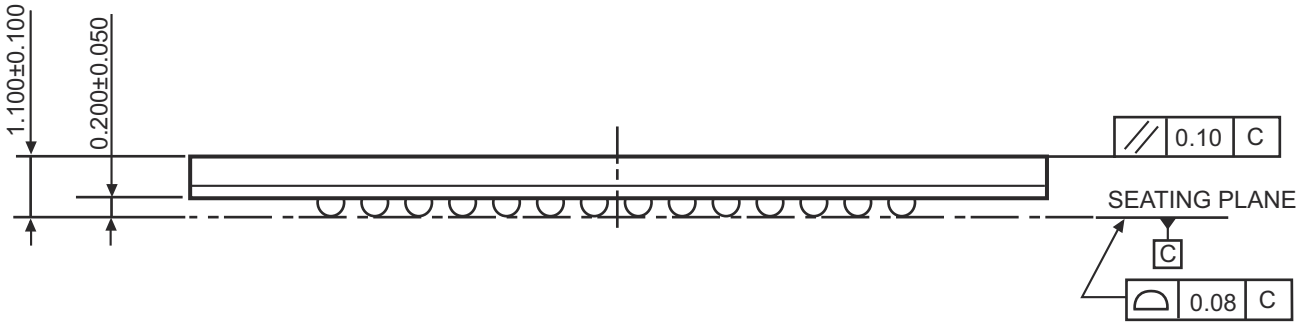


7-3) 12X16X1.0 (Bottom side)

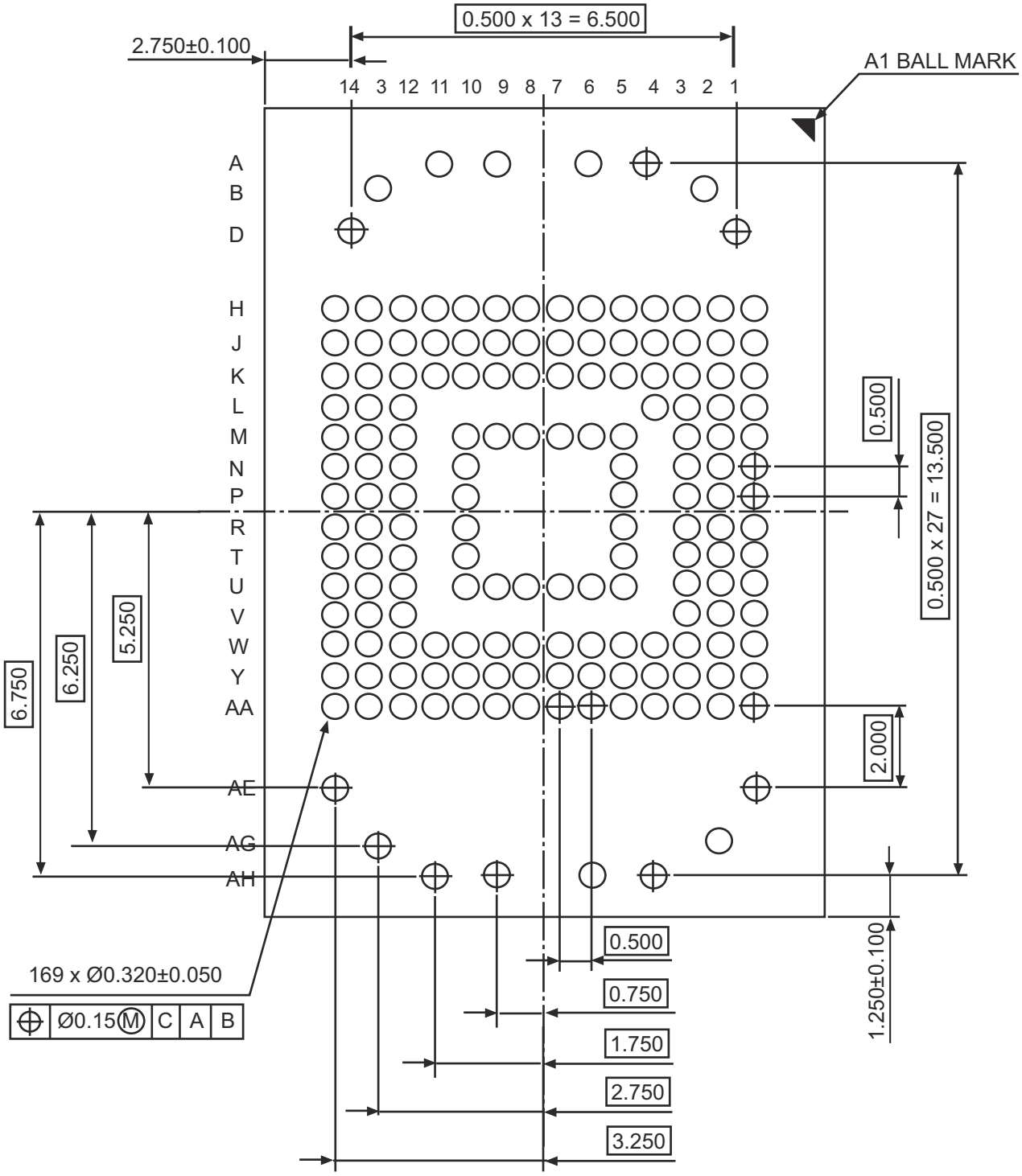


7-4) 12X16X1.2 (Top side)





7-4) 12X16X1.2 (Bottom side)



Appendix

1. Sleep mode current without NAND Power consumption

Density	Typical	Max	Unit
4/8/16/32GB	100	200	uA

Condition: VCCQ 1.8V, VCC 3.3V, Clock@52Mhz, 8bit bus width , Room temp

2. Standby current

Operation	Test condition	Typical	Max
Standby	**VCC=3.3V**±5%	40	200
	VCCQ=1.8V±5%	100	150

Condition: VCCQ 1.8V, VCC 3.3V, Clock@52Mhz, 8bit bus width , Room temp

3. Active current

Density	Typical	Max	Unit
4/8/16/32GB	100	200	mA

Condition1: VCCQ 1.8V, VCC 3.3V, Clock@52Mhz, 8bit bus width , Room temp
Condition2: Current measurements are average over 100mSec.
Condition3: The max active current is RMS, NOT peak current.

4. Wake up times from sleep (NAND power cut off)

Operation	Typical	Max	Unit
Wake up time	5	10	us

Condition: VCCQ 1.8V, VCC 3.3V, Clock 25Mhz, 8bit bus width , Room temp

5. Block read/write access time

Operation	Typical	Max	Unit
Block read	380	450	cycle
Block write	60	70	

Condition: VCCQ 1.8V, VCC 3.3V, Clock 25Mhz, 8bit bus width , Room temp

6. Initialization time (From CMD1 to ready)

Operation	Typical	Max	Unit
Initialization time	205	1000	ms

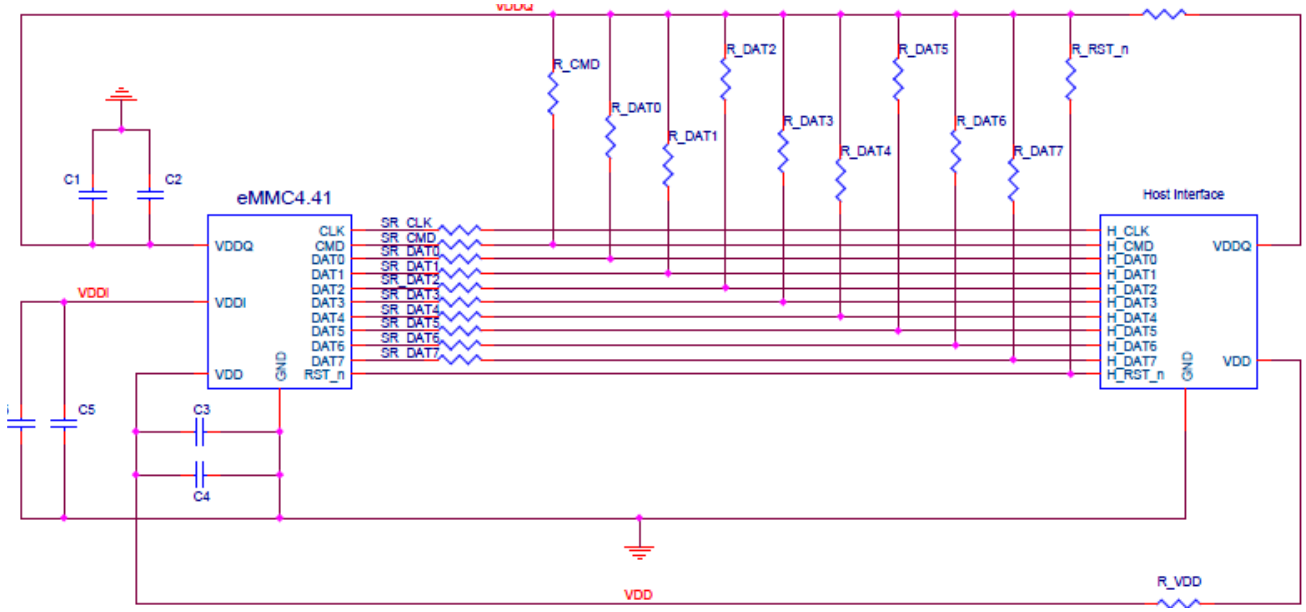
Condition: VCCQ 1.8V, VCC 3.3V, Clock 25Mhz, 8bit bus width , Room temp

7. System performance

System peroformance	Typical value(1)	Unit
Multiple block read sequential(2)		MB/s
Multiple block read 64KB chunk(3)		MB/s
Multiple block Write sequential(2)		MB/s
Multiple block Write 64KB chunk(3)		MB/s

1. Values given for an 8bit bus width, a clock frequency of 52MHz, VCC = 3.3V and VCCQ=1.8V
2. Based on a 4-Mbyte file transfer
3. Test performed by writing/reading a 64Kbyte chunk of data to/from random logical addresses of the card.

8. Connection guide



Parameter	Symbol	Min	Max.	Recommand	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	kohm	to prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10	50	50	kohm	to prevent bus floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	50	kohm	It is not necessary to put pull-up resistance on RST_n(H/W reset) line if host does not use H/W reset.
Impedence on CLK/CMD/ DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_CLK	0	47	22	ohm	
Serial's resistance on CMD/ DAT0~7 Line	SR_CMD SR_DAT0~7	0	47	0	ohm	
VDDQ Capacitor value	C1 & C2	2.2 + 0.1	4.7 + 0.22	2.2 +0.1	uF	Coupling capacitor should be connected with VDDQ and VSSQ as closely as possible
VDD Capacitor value($\leq$ 8GB)	C3 & C4	2.2 + 0.1	4.7 + 0.22	2.2 +0.1	uF	Coupling capacitor should be connected with VDD and VSS as closely as possible
VDD Capacitor value($\geq$ 8GB)	C3 & C4	2.2 + 0.1	4.7 + 0.22	4.7+0.22	uF	
VDDi capacitor value	C_{reg}	1	4.7 + 0.1	0.1	uF	Coupling capacitor should be connected with VDDi and VSSi as closely as possible

9. User data area size

Density	Sec_Count	Memory Capacity
4GB	00738000h	3696MB
8GB	00E74000h	7400MB
16GB	01D74000h	15080MB
32GB	TBD	

10. Boot & RPMB Size

Density	Boot partition 1	Boot partition 2	RPMB
4GB	2MB	2MB	2MB
8GB	2MB	2MB	2MB
16GB	4MB	4MB	4MB
32GB	TBD		

11. Erase unit & Write protect group size

Density	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	ERASE unit size(MB)	Write protect Group Size(MB)
4GB	08h	01h		
8GB	10h	01h	TBD	TBD
16GB	10h	02h		
32GB	TBD	TBD	TBD	TBD

12. Guideline for writing data into boot partition

In the most cases, write operation is executed only 1time and majority is read operation in boot partition.
Hynix e-NAND controller merges boot data after every write operation in order to reduce boot data access time.
(Hynix e-NAND boot data access time: typ: 65ms, max 150ms)
As a result, although host writes small chunk size data into boot partition, write time for it is not very different from large chunk size. So, it is highly recommended for host write as much as possible when writing data into boot partition.

Chunk size	2KB	64KB	512KB
Write time	220ms	247ms	262ms